

## CLAIMS

What is claimed is:

- 1 1. A method to design an integrated semiconductor product, comprising:
  - 2 (a) inputting a description of a range of processing functions into a slice description,
  - 3 the slice description comprising a transistor fabric, and/or at least one hardmac
  - 4 memory;
  - 5 (b) determining if the range of processing functions has a plurality of memory
  - 6 requirements; and
  - 7 (c) determining a largest common memory that can satisfy the range of processing
  - 8 functions and the plurality of memory requirements.

1 2. The method of claim 1, further comprising embedding the largest common memory into  
2 the at least one hardmac memory.

1 3. The method of claim 2, further comprising:  
2 (a) embedding at least one embodiment of the range of processing functions  
3 into the slice description.

1 4. The method of claim 1, further comprising:  
2 (a) generating register transfer logic from the transistor fabric so that one of  
3 the range of processing functions can use a first portion of the largest common  
4 memory.

1 5. The method of claim 4, wherein the register transfer logic further comprises  
2 logic for a port to access the first portion of memory used by the one of the  
3 range of processing functions.

1 6. The method of claim 5, wherein the first portion of the largest common memory  
2 to be used by one of the range of processing functions is an instruction cache.

1 7. The method of claim 6, wherein a second portion of the largest common memory  
2 to be used by one of the range of processing functions contains tags/addresses  
3 for instructions in the instruction cache.

- 1 8. The method of claim 6, wherein a second portion of the largest common memory  
2 to be used by one of the range of processing functions is a valid register  
3 indicating valid and/or invalid instructions in the instruction cache.
- 1 9. The method of claim 4, wherein the first portion of the largest common memory  
2 to be used by one of the range of processing functions is a data cache.
- 1 10. The method of claim 9, wherein a second portion of the largest common memory  
2 to be used by one of the range of processing functions contains tags/addresses  
3 for data in the data cache.
- 1 11. The method of claim 9, wherein a second portion of the largest common memory  
2 to be used by one of the range of processing functions is a valid register  
3 indicating which data in the data cache is or is not valid.
- 1 12. The method of claim 4, wherein a first portion of the largest common memory to  
2 be used by one of the range of processing functions is a tightly coupled memory.
- 1 13. The method of claim 4, further comprising:  
2 (a) identifying a second portion of the largest common memory not used by  
3 one of the range of processing functions;  
4 (b) generating register transfer logic to create an additional function from the  
5 transistor fabric;

6 (c) generating register transfer logic to create an additional register and/or  
7 memory from the second portion of the largest common memory;  
8 (c) generating the interconnect register transfer logic to connect the  
9 additional register and or memory to the additional function;  
10 (d) adding the interconnect and the generated register transfer logic to the  
11 slice description.

- 1 14. An article of manufacture, comprising a data storage medium tangibly embodying  
2 a program of machine readable instructions executable by an electronic  
3 processing apparatus to perform method steps for operating an electronic  
4 processing apparatus, said method steps comprising the steps of:  
5 (a) reading a plurality of input files relating to a plurality of embodiments of  
6 processing functions that could be incorporated into a design of a partially  
7 manufactured semiconductor product having a transistor fabric;  
8 (b) determining the largest common superset of memory that can be used by  
9 all of the plurality of embodiments of the processing function;  
10 (c) embedding the superset of memory into the design of the partially  
11 manufactured semiconductor product;  
12 (d) generating a plurality of output files to configure the embedded memory  
13 superset for use by a selected embodiment of the plurality of processing  
14 functions; and  
15 (e) updating the design of the partially manufactured semiconductor product  
16 with the output files.

1 15. The article of manufacture of claim 14, wherein the output files comprise  
2 register transfer logic to tie off any portion of the embedded memory superset not used  
3 by the selected embodiment of the plurality of processing functions.

1 16. The article of manufacture of claim 14, wherein the output files comprise  
2 register transfer logic to convert a portion of the transistor fabric to access the  
3 embedded memory superset used by the selected embodiment of the plurality of  
4 processing functions.

1 17. A method of configuring a partially manufactured semiconductor product having a  
2 transistor fabric and embedded with a memory superset capable of satisfying the  
3 memory/register requirements of all of a range of processing functions, the  
4 method of configuring comprising the steps of:

- 5 (a) selecting one processing function from the range of processing functions;
- 6 (b) determining how the memory superset is to be apportioned to the selected  
7 one processing function;
- 8 (c) apportioning the memory superset;
- 9 (d) tying off that portion of the memory superset that is not apportioned;
- 10 (e) determining how to access the apportioned memory superset;
- 11 (f) creating logic within the transistor fabric to access the apportioned  
12 memory superset.

1 18. A system to design a partially manufactured semiconductor product, comprising:

2 (a) means to receive a functional description of the partially manufactured  
3 semiconductor product;

4 (b) means to determine if the functional description may include a range of  
5 processing functions;

6 (c) means to evaluate the memory and/or register requirements of the range  
7 of processing functions;

8 (d) means to specify a memory superset configurable for a memory and/or  
9 register requirement for all of the processing functions in the range; and

10 (e) means to embed the memory superset into the partially manufactured  
11 semiconductor product.

1 19. The system of claim 18, further comprising:

2 (a) means to configure the memory superset into the memory and/or register  
3 requirement for one or more of the processing functions in the range;

4 (b) means to create the logic necessary to access the memory and/or register  
5 requirement for one or more of the processing functions in the range.

1 20. A partially manufactured semiconductor product, comprising:

2 (a) a plurality of functional areas, at least one of the functional areas  
3 embedded into the semiconductor product as a configurable superset of  
4 semiconductor memory;

5 (b) at least another of the functional areas reserved for one of a range of  
6 processing circuits, each one of the range of processing circuits capable of using  
7 all or a portion of the configurable superset of semiconductor memory;

8 (c) configuration logic capable of fulfilling a memory/register requirement of  
9 at least one of the range of processing circuits from the configurable superset of  
10 semiconductor memory; and

11 (d) port logic capable of accessing the memory/register requirement fulfilled  
12 from the configurable superset of semiconductor memory.